Listing of Claims

1. (Currently Amended) A method for managing ATM resources, comprising:

passing an ATM cell received by an ATM switch to a cell processing circuit, said passing including adding an α Byte of routing information to a header of the ATM cell;

removing the routing information added to the ATM cell after processing by the cell processing circuit; and

routing the ATM cell to a destination based on the removed routing information, wherein the routing information is added after the ATM cell passes through the ATM switch and wherein the ATM cell is routed along a signal path that bypasses the ATM switch after the routing information is removed.

2. (Currently Amended) A method of switching an asynchronous transfer mode (ATM) cell having a payload portion and a header portion comprising:

passing the ATM cell received through an ATM switch to a cell processing circuit, said passing including[[;]] adding [[an]] a destination information field to the header portion of the ATM cell;

processing the ATM cell; and

forwarding the ATM cell to a destination after the destination information field is removed, wherein the ATM cell is forwarded to said destination along a signal path that bypasses

the ATM switch and wherein the destination information field is added to the header portion by the ATM switch or a circuit located between the ATM switch and the cell processing circuit.

3. (Previously Presented) The method of claim 2, wherein the ATM cell during processing has (53+ α) bytes, and α corresponds to a size of the information field.

4. (Canceled)

5. (Currently Amended) A method of processing an asynchronous transfer mode (ATM) cell comprising:

switching a received ATM cell through an ATM switch;

adding routing information in a header of the ATM cell that has been switched; and

forwarding the ATM cell according to the added routing information ~~without any further cell switching~~ to a destination based on the routing information added to the header of the ATM cell ~~through the ATM switch~~, wherein routing information is removed from the ATM cell ~~being~~ and the ATM cell is forwarded to the destination along a signal path that bypasses the ATM switch, and wherein the destination information field is added to the header portion by the ATM switch or a circuit located between the ATM switch and the cell processing circuit.

6. (Original) The method of claim 5, wherein the received ATM cell has a size of 53 bytes.

7. (Original) The method of claim 6, wherein the added routing information has a size of 1 byte.

8. (Original) The method of claim 7, wherein the forwarded ATM cell has a size of 53 bytes, after the 1 byte routing information has been removed.

9. (Previously Presented) The method of claim 5, further comprising processing the ATM cell before forwarding.

10. (Currently Amended) The method of claim 9, wherein said processing comprises changing of an ATM adaptation layer (AAL) type or a changing of payload information.

11. (Previously Presented) An asynchronous transfer mode (ATM) cell switching system comprising:

a first memory to receive and store an ATM cell to be handled;

a cell switching unit to receive the ATM cell stored in the first memory, and to assign an appropriate path for the ATM cell to be forwarded ~~to~~; ~~and~~

a second memory to receive and store the ATM cell having the appropriate path assigned thereto from the cell switching unit;

a cell processor to receive and process the ATM cell from the second memory; and

a third memory to receive and store the ATM cell processed by the cell processor and to output the ATM cell without going through the cell switching unit.

12. (Canceled)

13. (Previously Presented) The system of claim 11, wherein the cell switching unit provides an output to a physical layer and to a loop back, or an output for further processing.

14. (Previously Presented) The system of claim 13, wherein the cell switching unit adds an end destination field in a header of the ATM cell.

15. (Previously Presented) The system of claim 14, wherein the added end destination field is maintained as the ATM cell passes through the second memory, the cell processor and the third memory.

16. (Previously Presented) The system of claim 15, wherein the third memory outputs the ATM cell directly to a physical layer or to a loop back in accordance with information included in the end destination field.

17. (Original) The system of claim 11, wherein the cell switching unit requires a one virtual path identifier/virtual channel identifier (VPI/VCI) and one type of routing information for any received ATM cell.

18. (Currently Amended) The system of claim 11 [[12]], wherein the cell processor processes the received ATM cell by changing an ATM adaptation layer (AAL) type or by changing payload information.

19-21 (Canceled)

22. (Previously Presented) The method of claim 1, wherein processing by the cell processing circuit includes at least one of changing an ATM adaptation layer type or changing payload information.

23. (Previously Presented) The method of claim 1, wherein the routing information included in the α Byte identifies one of the following as a destination of the ATM cell: one of a plurality of physical connections or a loop-back path of a network.